IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#8

In re Patent Application of)
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ELIYAHOU HARARI, ROBERT D.)
NORMAN and SANJAY MEHROTRA)
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Serial No.: 09/143,233)
)
Filed: August 28, 1998)
)
For: FLASH Eeprom SYSTEM)
_____)

Group Art Unit: 2785

Examiner: L. Hua

San Francisco, California

Assistant Commissioner of Patents
Washington, D.C. 20231

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner of Patents, Washington, D.C. 20231 on April 28, 1999.

Brenda J. Dolly

Brenda J. Dolly Apr. 28, 1999
Signature Date

RESPONSE TO OFFICE ACTION
AND
REQUEST FOR DECLARATION OF INTERFERENCE

Sir:

This is in response to the Office Action dated December 31, 1998, in the above-referenced patent application, and further requests that an interference be declared between the present application and patent no. 5,668,763 to Fujioka et al.

Reconsideration of the rejection of the claims of the present application on the ground of double patenting with patent no. 5,297,148, which is a parent to the present application, is respectfully requested. Claim 1 of the cited '148 patent and claim 63 of the present application, having the broadest scope in each of the respective patent and application, do not overlap or cross-read on one another. Each of these claims contains limitations not included in the other. For

example, claim 63 of the present application specifies that the memory blocks are organized into a plurality of memory arrays, a limitation not found in the '148 patent claim 1. Conversely, the '148 patent claim 1 defines a memory card with its sectors including redundant cells, a memory controller, a defective cell detector, a defect pointer and a defective cell substituting means, none of which are limitations expressed in claim 63 of the present application. Claim 1 of the '148 patent is quite specific to handling defective cells within individual sectors by replacing them with redundant cells within the same sectors, subject matter quite distinct from the block (sector) substitution across a plurality of memory arrays that is defined by claim 63 of the present application. Further, there has been no showing that the difference between the two claims would have been obvious to one ordinarily skilled in the art, as would be required to sustain an obviousness type of double patenting rejection.

Reconsideration of the rejection of the claims of the present application under 35 U.S.C. §103(a) is also respectfully requested. This obviousness rejection is based upon a combination of U.S. patents nos. 4,475,194 to LaVallee et al. and 4,989,181 to Harada. However, the Harada patent is not early enough to be prior art against the present application, and the LaVallee et al. patent is of record in the patent no. 5,668,763 to Fujioka et al., from which the present rejected application claims were copied. The Harada patent can be prior art under 35 U.S.C. §103(a), as defined by 35 U.S.C. §102(e), only as of its U.S. filing date of May 30, 1989, which is after the April 13, 1989 effective filing date of the present application. The present application is one of a chain of continuation and divisional applications that goes back to the original application serial no. 07/337,566, filed April 13, 1989. The Harada patent is not prior art under 35 U.S.C. §102(e) as of its Japanese priority application filing date. (See M.P.E.P. §2136.02, page 2100-84, July 1998.) The LaVallee et al. patent was not used to form a rejection of claims by the Examiner during the prosecution of patent no. 5,668,763 to Fujioka et al., a review of its file history revels, but rather it was first cited by the Examiner with other references at the time the application was allowed.

Further, it should be noted that since the present application claims are exact copies of claims from the Fujioka et al. patent no. 5,668,763, the USPTO procedure is to require approval of the Group Director before rejecting the claims on a ground also applicable to the patent. (See M.P.E.P. §2307.02, page 2300-13, July 1998.) In this case, since the Fujioka et al. patent no.

5,668,763 was filed only in 1996, many years after the 1989 effective filing date of the present application, the prior art cited in the present application would be applicable to that patent.

REQUEST FOR DECLARATION OF INTERFERENCE

An interference proceeding between the present application and the Fujioka et al. patent no. 5,668,763 is solicited. Claim 63 of the present application, corresponding to claim 1 of the Fujioka et al. patent no. 5,668,763, is proposed as the single count of the interference, as follows:

Proposed Interference Count 1

A semiconductor memory selectively enabled for operation as a complete operative memory or a partial operative memory, comprising:

a plurality of memory arrays, each memory array comprising a plurality of memory blocks; and

a plurality of selection circuits respectively associated with said plurality of memory arrays, selectively and independently disabling a defective memory block and selecting a normal memory block of a memory array for enabling operation thereof as a partial operative memory.

35 U.S.C. 135(b)

Claim 63 of the present application was added by a Preliminary Amendment filed concurrently with the present continuation application, namely on August 28, 1998. This is less than one year after the Fujioka et al. patent no. 5,668,763 was granted on September 16, 1997.

Effective Filing Date

As specified in the "Cross-Reference to Related Application" section added to the beginning of the present application by the Preliminary Amendment filed with it on August 28, 1998, the present application is entitled to an effective filing date of April 13, 1989.

The Fujioka et al. patent no. 5,668,763 appears to have an earliest effective United States filing date of February 26, 1996. This is over five years after the April 13, 1989 effective filing date of the present application.

Therefore, it is requested that the interference be declared with the Applicant of the present application designated as the senior party.

Inventorship

As a result of preparing the present interference request, it has been recognized that less than all the inventors named in the present application are properly named inventors of the subject matter now claimed. Accordingly, an accompanying Amendment is being filed under 37 C.F.R. 1.48(b) to delete two of the three inventors from this application, leaving Dr. Eliyahou Harari as the sole named inventor.

Support for the Proposed Count 1 in the Present Application

The outstanding Office Action in the present application expressly recognizes that the subject matter claimed in the present application is fully disclosed by U.S. patent no. 5,297,148. (Office Action, page 2, ¶2, ln. 4.) Patent no. 5, 297,148 is a parent in the chain of patents leading to the present application, having the same disclosure as that of the present application.

Information Disclosure Statement

A Supplemental Information Disclosure Statement is being filed herewith to list the references cited in the Fujioka et al. patent no. 5,668,763, and those cited in applications related to the present one.

Conclusion

A prompt declaration of the requested interference is respectfully requested.

Dated: April 28, 1999

Respectfully submitted,

Gerald P. Parsons

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